WHAT IS CLAIMED IS:

1. A driver circuit for a display device comprising:

a shift register circuit having a plurality of register circuits including a clocked inverter circuit and an inverter circuit connected in series;

a plurality of digital data latch circuits having a first N-channel transistor and a second N-channel transistor in which the sources or drains are connected in series, a P-channel transistor, and

a digital data holding circuit, wherein:

said clocked inverter circuit and said inverter circuit generate a timing signal on the basis of a clock signal, a clock back signal, and a start pulse inputted from outside, and feeds the timing signal to a register circuit neighboring said register circuit and a gate electrode of said second N-channel transistor;

said P-channel transistor inputs a first electric current voltage to said digital data holding circuit in accordance with a reset signal that is inputted from outside to a gate electrode of the P-channel transistor;

said first N-channel transistor takes in digital data inputted on the basis of said timing signal and feeds the digital data to the source or the drain of the second N-channel transistor; and

the timing signal outputted from a register circuit neighboring said register circuit is fed to a gate electrode of said first N-channel transistor.

2. A driver circuit for a display device according to claim 1, wherein the digital data holding circuit has two inverter circuits.

3. A driver circuit for a display device according to claim 1, wherein the digital data holding circuit has a capacitance.

4. Electronic equipment comprising a display device according to claim 1 is selected from the group consisting of a projector, rear projector, front projector, goggle type display, mobile computer, notebook personal computer, video camera, DVD player, and game machine.

5. A driver circuit for a display device comprising:

a shift register circuit having a register circuit including a clocked inverter circuit and an inverter circuit connected in series;

a digital data latch circuit having a first N-channel transistor and a second N-channel transistor in which the sources or drains are connected in series, a P-channel transistor, and a digital data holding circuit, wherein:

a gate electrode of said second N-channel transistor is connected to the output line of said register circuit, a source or a drain of said second N-channel transistor is connected to a source or a drain of said first N-channel transistor, and the other end of the source or the drain

of the said second N-channel transistor is connected to said digital data holding circuit;

a gate electrode of said first N-channel transistor is connected to the output line of a register circuit neighboring said register circuit and the other end of the source or the drain of said first N-channel transistor is connected to a signal line to which digital data are inputted; and

a gate electrode of said P-channel transistor is connected to a signal line to which a reset signal is inputted and one end of a source or a drain of said P-channel transistor is connected to a first power source whereas the other end of the source or the drain of the P-channel transistor is connected to said digital data holding circuit.

6. A driver circuit for a display device according to claim 5, wherein the digital data holding circuit has two inverter circuits.

7. A driver circuit for a display device according to claim 5, wherein the digital data holding circuit has a capacitance.

8. Electronic equipment comprising a display device according to claim 5 is selected from the group consisting of a projector, rear projector, front projector, goggle type display. mobile computer, notebook personal computer, video camera, DVD player, and game machine.

9. A driver circuit for a display device comprising:

a shift register circuit having a plurality of register circuits including a clocked inverter circuit and an inverter circuit connected in series;

a plurality of digital data latch circuits having a first P-channel transistor and a second P-channel transistor in which the sources or drains are connected in series, an N-channel transistor, and

a digital data holding circuit, wherein:

said clocked inverter circuit and said inverter circuit generate a timing signal on the basis of a clock signal, a clock back signal, and a start pulse inputted from outside and feeds the timing signal to a register circuit neighboring said register circuit and to a gate electrode of said second P-channel transistor;

said N-channel transistor feeds a second electric current voltage to said digital data holding circuit in accordance with a reset signal that is inputted from outside to a gate electrode of said N-channel transistor;

said first P-channel transistor takes in digital data inputted on the basis of said timing signal and feeds the digital data to the source or the drain of said second P-channel transistor; and

the timing signal outputted from a register circuit neighboring said register circuit is fed to a gate electrode of said first P-channel transistor.

10. A driver circuit for a display device according to claim 9, wherein the digital data

holding circuit has two inverter circuits.

11. A driver circuit for a display device according to claim 9, wherein the digital data holding circuit has a capacitance.

12. Electronic equipment comprising a display device according to claim 9 is selected from the group consisting of a projector, rear projector, front projector, goggle type display, mobile computer, notebook personal computer, video camera, DVD player, and game machine.

13. A driver circuit for a display device comprising:

a shift register circuit having a register circuit including a clocked inverter circuit and an inverter circuit connected in series;

a digital data latch circuit having a first P-channel transistor and a second P-channel transistor in which the sources or drains are connected in series, an N-channel transistor, and

a digital data holding circuit, wherein:

a gate electrode of said second P-channel transistor is connected to the output line of said register circuit, a source or a drain of said second P-channel transistor is connected to a source or a drain of said first P-channel transistor, and the other end of the source or the drain of the said second P-channel transistor is connected to said digital data holding circuit;

a gate electrode of said first P-channel transistor is connected to the output line of a

register circuit neighboring said register circuit and the other end of the source or the drain of said first P-channel transistor is connected to a signal line to which digital data are inputted; and

a gate electrode of said N-channel transistor is connected to a signal line to which a reset signal is inputted and one end of a source or a drain of said N-channel transistor is connected to a second power source whereas the other end of the source or the drain of the N-channel transistor is connected to said digital data holding circuit.

14. A driver circuit for a display device according to claim 13, wherein the digital data holding circuit has two inverter circuits.

15. A driver circuit for a display device according to claim 13, wherein the digital data holding circuit has a capacitance.

16. Electronic equipment comprising a display device according to claim 13 is selected from the group consisting of a projector, rear projector, front projector, goggle type display, mobile computer, notebook personal computer, video camera, DVD player, and game machine.